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Design a Low-Jitter Clock for High-Speed Data Converters

High-speed applications using ultra-fast data converters in their design often require an extremely clean clock signal to make sure an external clock source does not contribute undesired noise to the overal dynamic performance of the system. It is therefore crucial to select suitable system components, which help generate a low phase-jitter clock. The following application note serves as a valuable guide for selecting the appropriate components to design a low-phase noise PLL-based clock generator, suitable for ultra-fast data converters.

Introduction

Many modern, high-speed, high-performance integrated circuits, such as the MAX104 and MAX106 analog-to-digital converters (ADCs), require a low-phase-noise (low-jitter) clock that operates in the GHz range. Conventional crystal oscillators may provide a low-jitter clock signal, but are not generally available in oscillating frequencies above 120MHz

Figure 1 illustrates the simplified block diagram of a typical high-speed data converter system. The system consists of a bandpass filter, ADC, high-frequency clock, high-speed storage device, and post processing unit. Aside from the MAX104, the high-frequency clock plays a significant role in determining the accuracy of a high-speed data converter. This high frequency, low-phase-noise clock is a combination of a high frequency voltage-controlled oscillator (U1), a phase-locked loop (U2), and a crystal oscillator (U3) as shown in Figure 2.

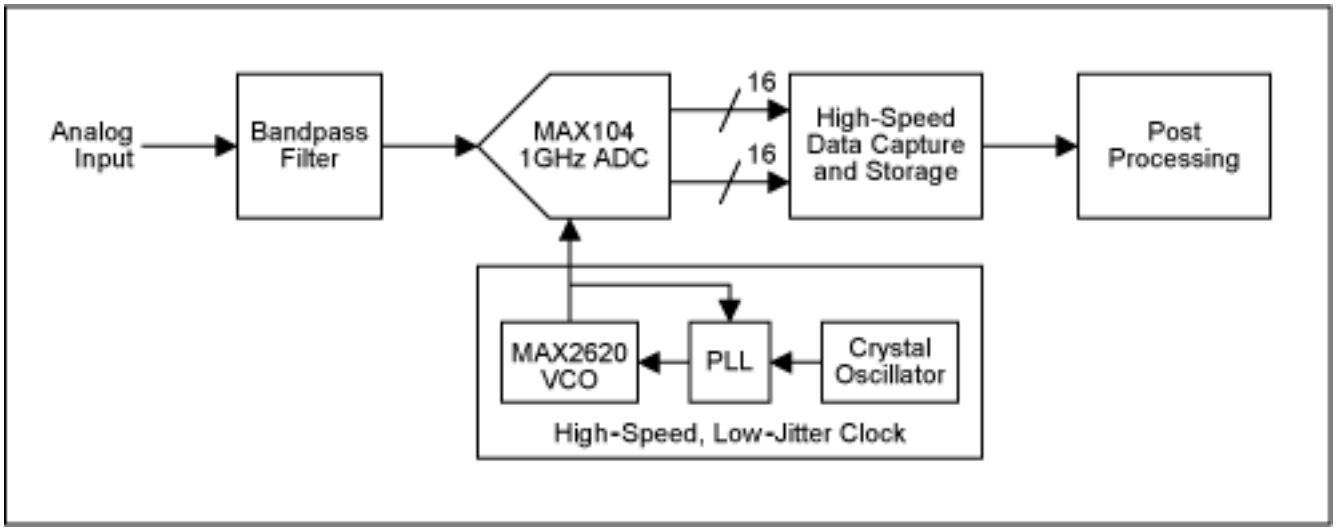

Figure 1. Typical high-speed data converter system using the MAX104 ADC and a PLL-based, low-jitter clock.

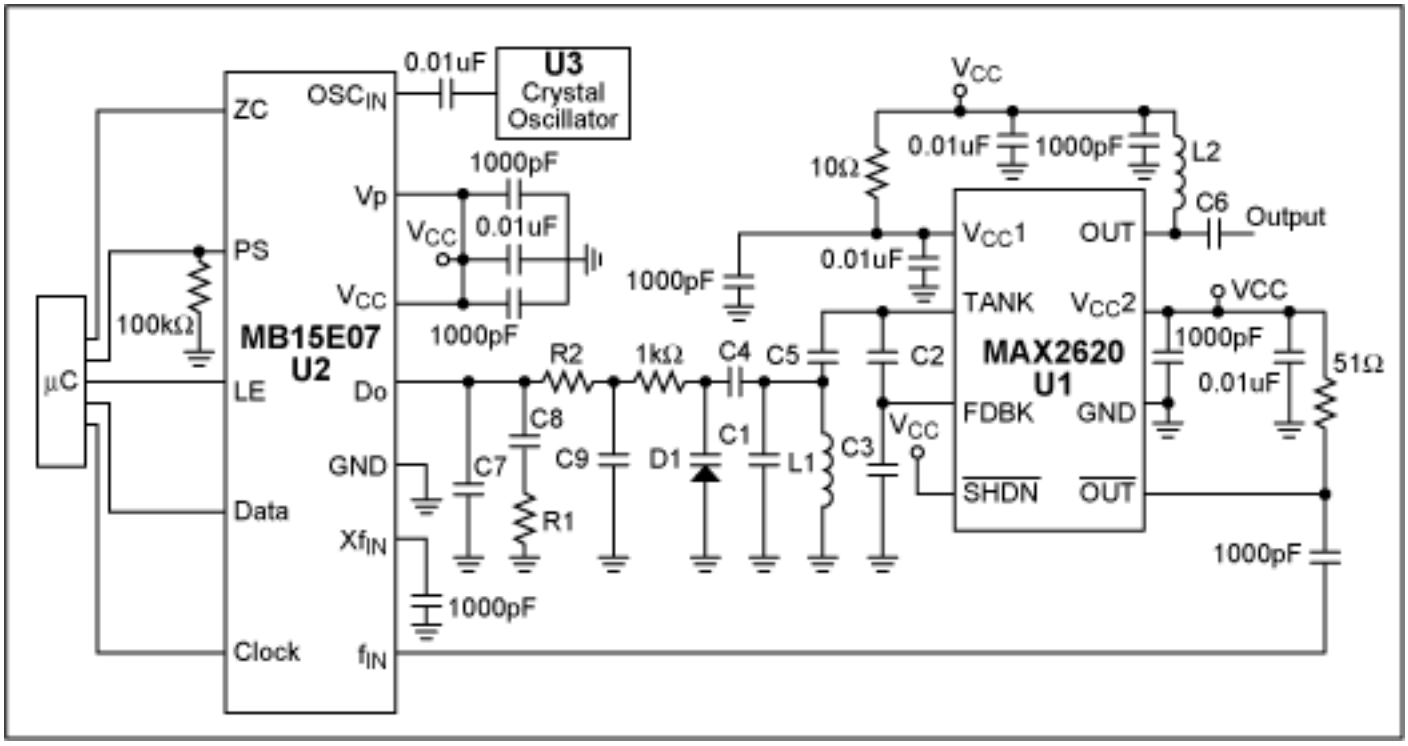

Figure 2. A high-speed, low-phase-noise clock is one of the most critical elements to ensure optimum dynamic performance of the high-speed ADC.

The MAX2620 voltage-controlled oscillator (VCO) is capable of generating oscillator frequencies up to 1GHz, while providing sufficient noise performance. Because of the inherent frequency drift, a phase-locked loop (PLL) is often required to lock the VCO output to the desired frequency by comparing the VCO output to a crystal oscillator frequency.

Choosing an appropriate VCO for a high-speed data converter system is not as simple as finding one with the right oscillator frequency. One key parameter that must be taken into

consideration is clock jitter. Jitter is generally defined as short-term, non-cumulative variation of the significant instant of a digital signal from its ideal position in time [6]. Figure 3 illustrates a sampling clock signal that contains jitter. Jitter generated by the clock is caused by various internal noise sources, such as thermal noise, phase noise, and spurious noise. In the case of a data converter, jitter affects the signal-to-noise ratio (SNR) performance of the data converter.

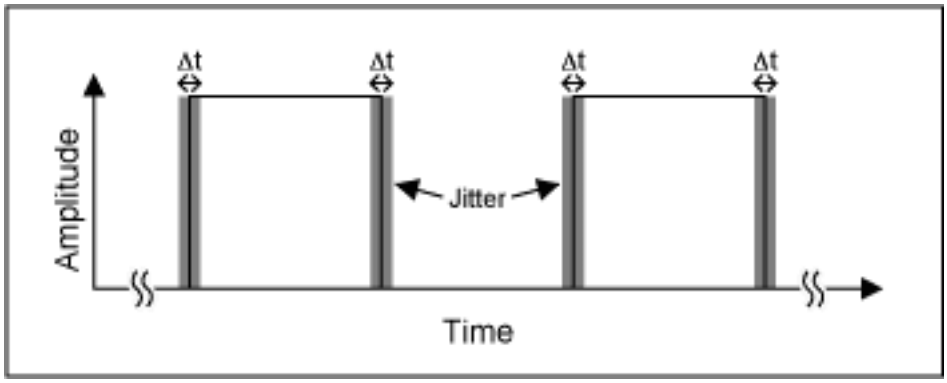

Figure 3. Jitter in clock signal degrades the ADC signal-to-noise ratio.

How Clock Jitter Degrades ADC's Signal-to-Noise Ratio (SNR)

Jitter generated by a clock source can cause the ADC's internal circuitry to falsely trigger the sampling time. As shown in Figure 4, uncertainty in sampling time Δt equates to uncertainty in amplitude ΔA [1]. This results in false sampling of the analog input amplitude, thus degrading the SNR of the ADC. With the following equations, the maximum SNR of a data converter can be calculated for a given amount of clock jitter:

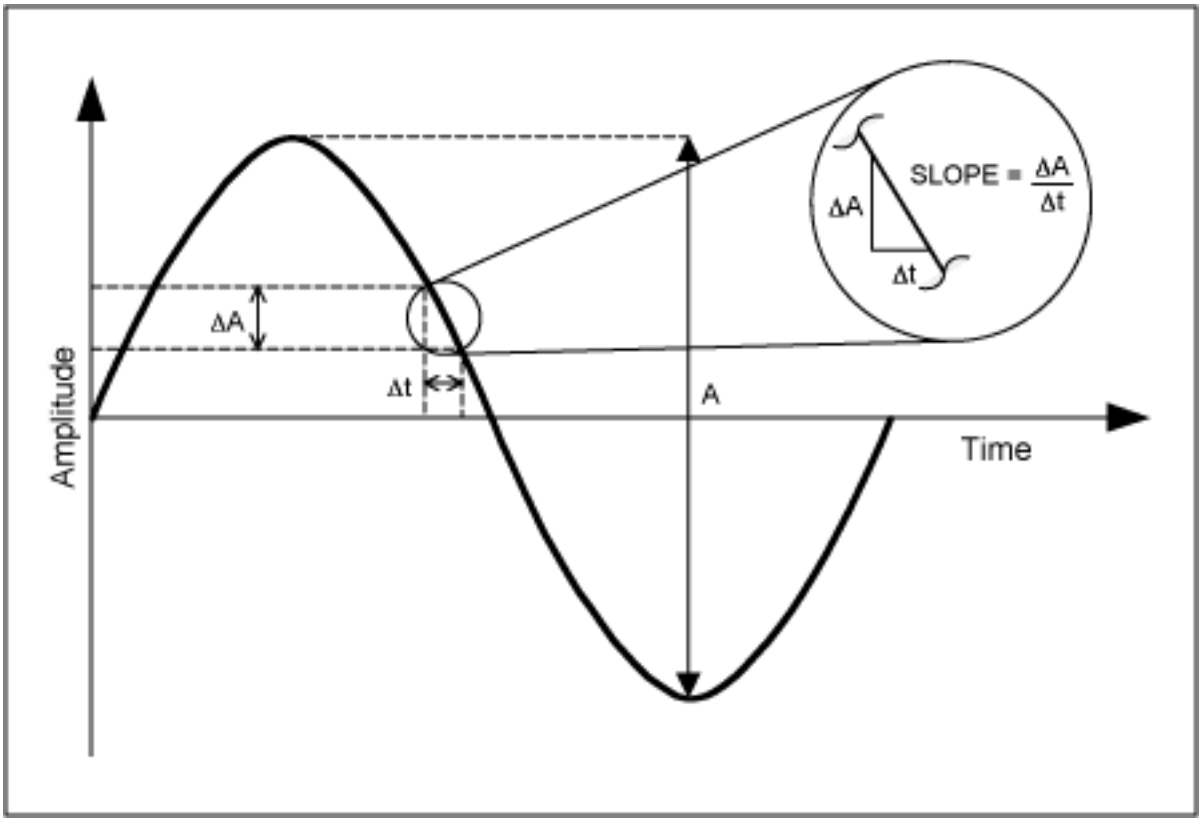

Figure 4. An SNR model obtained using the sampling time uncertainty.

$$\frac{\Delta A}{\Delta t} = \text{slope} = A\omega \cos(\omega t) \qquad \text{EQ. 1}$$

The slope is at its maximum when the term $\cos(\omega t) = 1$. Therefore,

$$\frac{\Delta A}{\Delta t} = A\omega \qquad \text{EQ. 2}$$

EQ.2 can be rearranged as:

$$\frac{A}{\Delta A} = \frac{1}{\Delta t \omega} \qquad \text{EQ. 3}$$

By definition, $A/(\Delta A)$ is the signal-to-noise ratio, and Δt is the root-mean-square (RMS) value of the jitter. EQ. 3 can be rewritten as:

$$SNR_{ADC} = \frac{1}{\sigma_{RMS}\omega} = \frac{1}{2\pi f \sigma_{RMS}} \qquad \text{EQ. 4}$$

For example, if the analog input signal is 250MHz, and 50dB SNR is to be achieved, the maximum RMS jitter (σ_{RMS}) must be less than 2ps.

How Noise Sources Cause Jitter

Thermal noise, frequency modulation (FM), amplitude modulation (AM), phase modulation (PM), and spurious components contribute to the noise that causes jitter in the clock signal. Because of the difficulty to distinguish noise caused by FM, AM, and PM, all three types of noise are grouped into a general term known as phase noise. To clarify the calculation of phase noise, a high frequency circuit, using the MAX2620 VCO and PLL, will be used as example.

Thermal Noise Contribution to Jitter

Figure 5 depicts a simplified plot of the VCO phase noise profile. The MAX2620's output amplifier has a thermal noise floor of approximately -147dBm/Hz. This noise is white, Gaussian noise with a finite bandwidth. Although the effective bandwidth has not been characterized, it can be approximated to be twice the operating frequency. With the MAX2620 properly tuned to the desired output frequency, the contribution of the noise floor to jitter can be computed with the following equation:

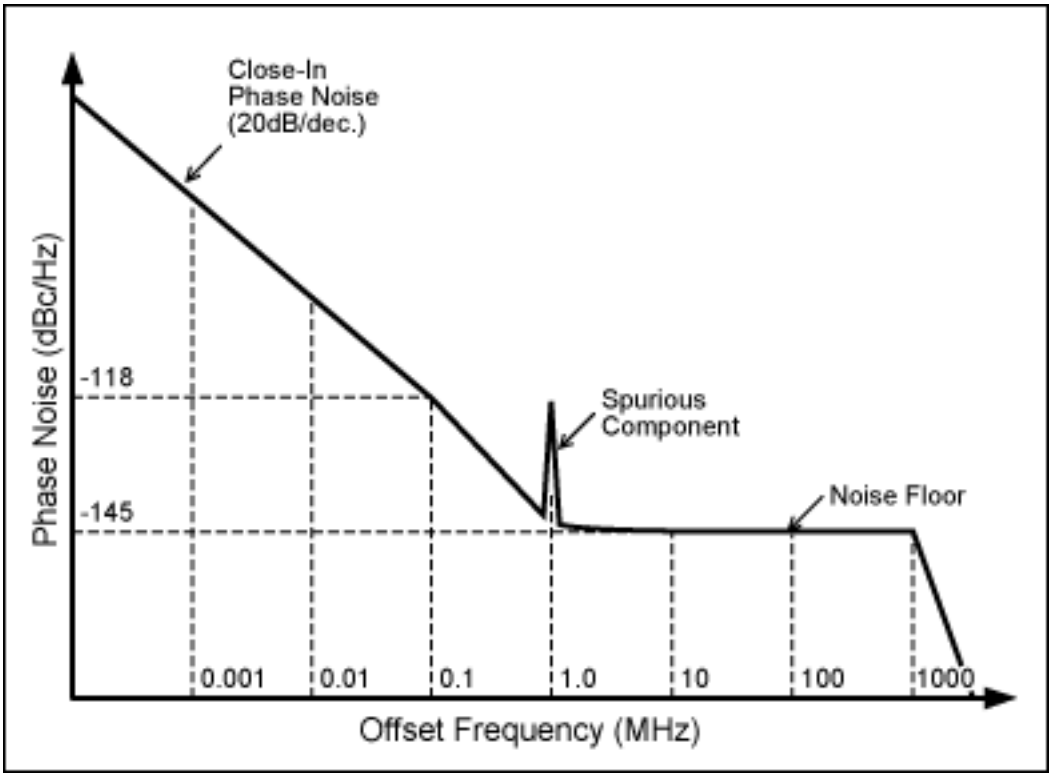

Figure 5. Simplified phase noise profile of the MAX2620 VCO as a function of the offset frequency.

$$\sigma_\tau^2 = \frac{8}{\omega_o^2}\int_0 L(f)\sin^2(\pi f\tau)df \qquad \text{EQ. 5}$$

σ_τ^2 = Edge-to-Edge Jitter Variance (in s_2)
$\omega_o = 2\pi f_o$ = Angular clock oscillation (center) frequency (in rad/s)
f_o = Oscillator (center) frequency (in Hz)
f = Offset frequency from the center frequency (in Hz)
$\tau = 1/2f_o$ = Half of a period (in s)
L(f) = Phase noise at offset frequency f (in dBc/Hz).

For further improvement in the noise performance, a power matching network (L2 and C6) whose frequency response similar to a bandpass filter is often applied at the VCO output. This attenuates undesired noise outside the bandwidth of interest. By doing so, one can estimate the worst noise by the limit of integration from 0Hz offset to f_0. Noise beyond these limits is greatly attenuated and can be ignored. Because the noise floor is even for offset frequencies from 0Hz to f_0, L(f) can be considered constant. EQ. 5 can be reduced to:

$$\sigma_\tau^2 = \frac{8L}{\omega_o^2}\int_0^{f_o}\sin^2(\pi f\tau)df \qquad \text{EQ. 6}$$

$$\sigma_\tau^2 = \frac{8L}{\omega_o^2}\left[\frac{2\pi\tau f - \sin(2\pi\tau f)}{4\pi\tau}\right]_0^{f_o} \qquad \text{EQ. 7}$$

$$\sigma_\tau^2 = \frac{4f_oL}{\omega_o^2} \qquad \text{EQ. 8}$$

The edge-to-edge timing jitter due to the noise floor is:

$$\sigma_\tau = \frac{2\sqrt{Lf_o}}{\omega_o} = \frac{2\sqrt{10^{-145/10}(1\cdot10^9)}}{2\pi(1\cdot10^9)} = 0.566\text{ps} \qquad \text{EQ. 9}$$

Because thermal noise is non-correlated, jitter is non-accumulated. The period-to-period jitter is the same as edge-to-edge jitter.

Equation 8 can also be displayed as:

$$\sigma_\tau^2 = \frac{2}{\omega_o^2} \frac{1}{SNR_{OSC}}, \quad \text{EQ. 10}$$

where SNR_{OSC} is the signal-to-noise ratio of the oscillator due to the noise floor.

Phase Noise Contribution to Jitter

Phase noise is characterized as the ratio of noise power at an offset frequency to the power level of the clock (carrier) signal. This ratio is usually normalized to 1Hz-bandwidth, resulting in a unit of dBc/Hz. For instance, the phase noise at 100kHz offset in Figure 5 is -118dBc. That means the noise power at 1000.1MHz is 118dB below the carrier power level at 1000MHz in 1Hz-bandwidth.

The free running phase noise of the MAX2620 is approximately 20dB/decade from the corner-offset frequency of 1MHz to the clock frequency. With EQ. 11, the period-to-period jitter due the phase noise can be calculated [5] as follows:

$$\sigma_\tau = \frac{f}{f_o^{1.5}} 10^{L(f)/20} = \frac{(100kHz)}{(1GHz)^{1.5}} 10^{-118/20} = 0.004ps, \quad \text{EQ. 11}$$

where f is the offset frequency from the clock frequency, and it has to be in the region where the phase noise decreases 20dB per decade. The phase noise, L(f), was taken from the MAX2620 characterization at f = 100kHz offset frequency. With f = 10kHz, the resulting jitter will not change.

Spurious Components Contribution to Jitter

A PLL-based clock signal produces spurs. If these spurs are not suppressed, they can degrade the jitter performance. Figure 6 shows a spectrum plot of a 1GHz clock signal taken with a spectrum analyzer. The two symmetrical pairs of spurs displayed in this figure are approximately 75dBc and 85dBc below the carrier. The separation of these spurs from the carrier and from each other is determined by the comparison frequency used in the phase-locked loop. In this case, the comparison frequency is 1MHz; therefore, the two spurs next to the carrier are exactly 1MHz away from the carrier and the subsequent pair. In addition, there is another pair of -75dBc spurs (not shown) at 20MHz offset caused by the crystal oscillator. The following equation, translates these spurs into jitter [6]:

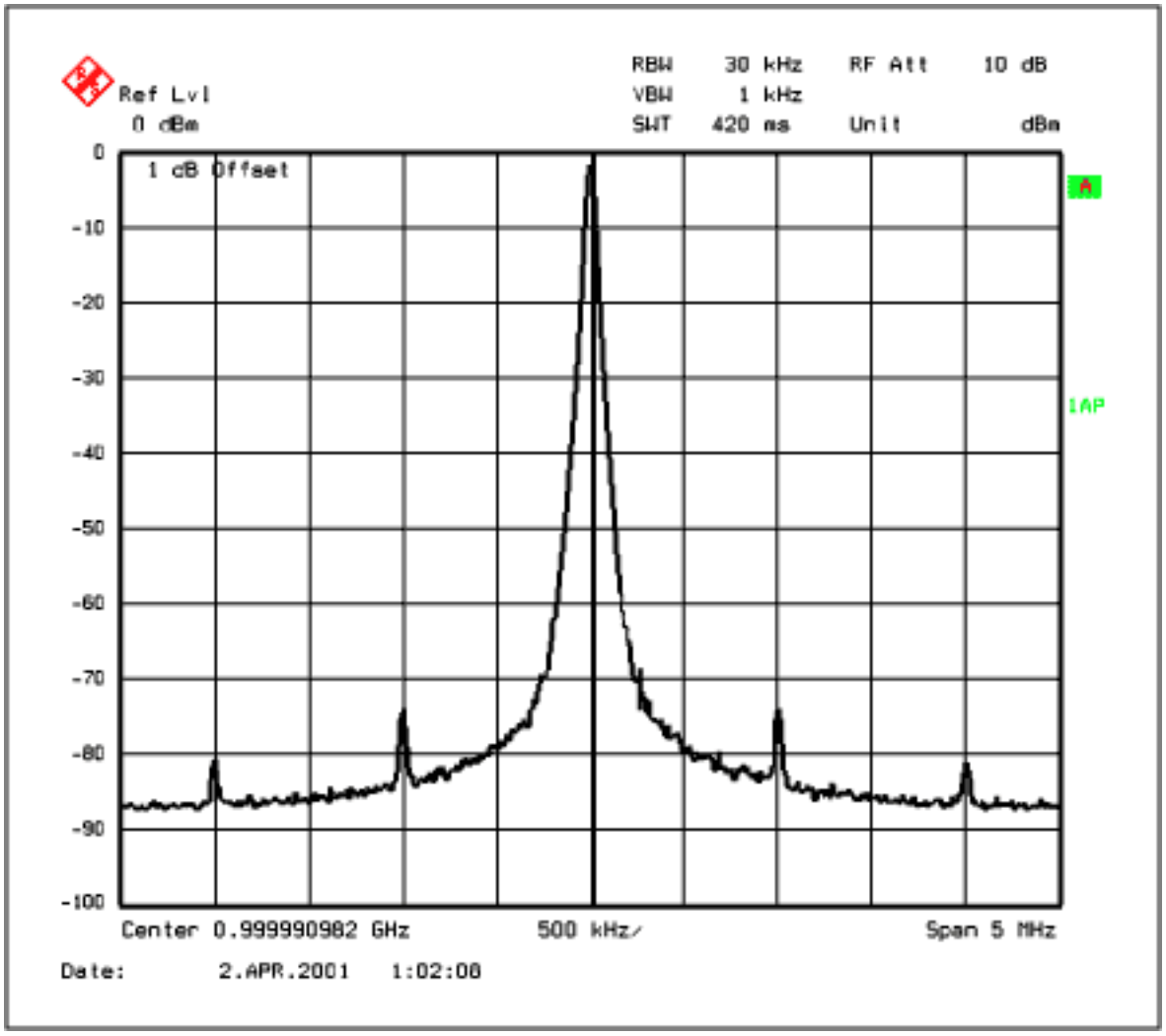

Figure 6. A 1GHz clock shown with spurious components.

$$\sigma_\tau^2 = \frac{8}{\omega_0^2} L(f_m)\sin^2\left[\pi f_m(m\tau)\right], \qquad \text{EQ. 12}$$

where f_m is offset frequency at which the phase noise spurious components occurred. With m = 1, the cycle-to-cycle jitter computes to 4.38×10^{-6}ps. For practical applications with ADCs, such as the MAX104, jitter due to spurious noise at this level is negligible.

Total Jitter

The total cycle-to-cycle jitter is a function of the square root of the sum of the jitter squares and can be calculated as follows:

$$\sigma_{total} = \sqrt{\sigma_{floor}^2 + \sigma_{phase\_noise}^2 + \Sigma\sigma_{spurious}^2} \quad \text{EQ. 13}$$

$$\sigma_{total} = \sqrt{(0.566 \cdot 10^{-12})^2 + (4 \cdot 10^{-15})^2 + (4.38 \cdot 10^{-18})^2 + (1.38 \cdot 10^{-18})^2} = 0.566ps$$

Phase-Locked Loop

As a result of inherit frequency drift due to temperature, power supply, load, etc., a free running VCO is rarely used by itself. Usually a phase-locked loop is introduced to help lock the VCO output to the desired frequency. If designed properly, the phase-locked loop can help reduce the phase noise. The phase noise within the loop bandwidth is lower than that of a free running VCO. Thus, the actual jitter due to phase noise is less than that of EQ. 11.

Figure 7 shows the functional diagram of the MB15E07 [7] in an integer-N PLL system. It consists of a phase detector (or comparator), an output charge-pump, a dual modulus pre-scalar, an N counter, and an R counter. The N counter consists of a main (M) counter and a swallow or auxiliary (A) counter.

$$N = PM + A, \quad (A < M) \quad \text{EQ. 14}$$

The N counter then works in conjunction with the dual modulus pre-scalar (P).

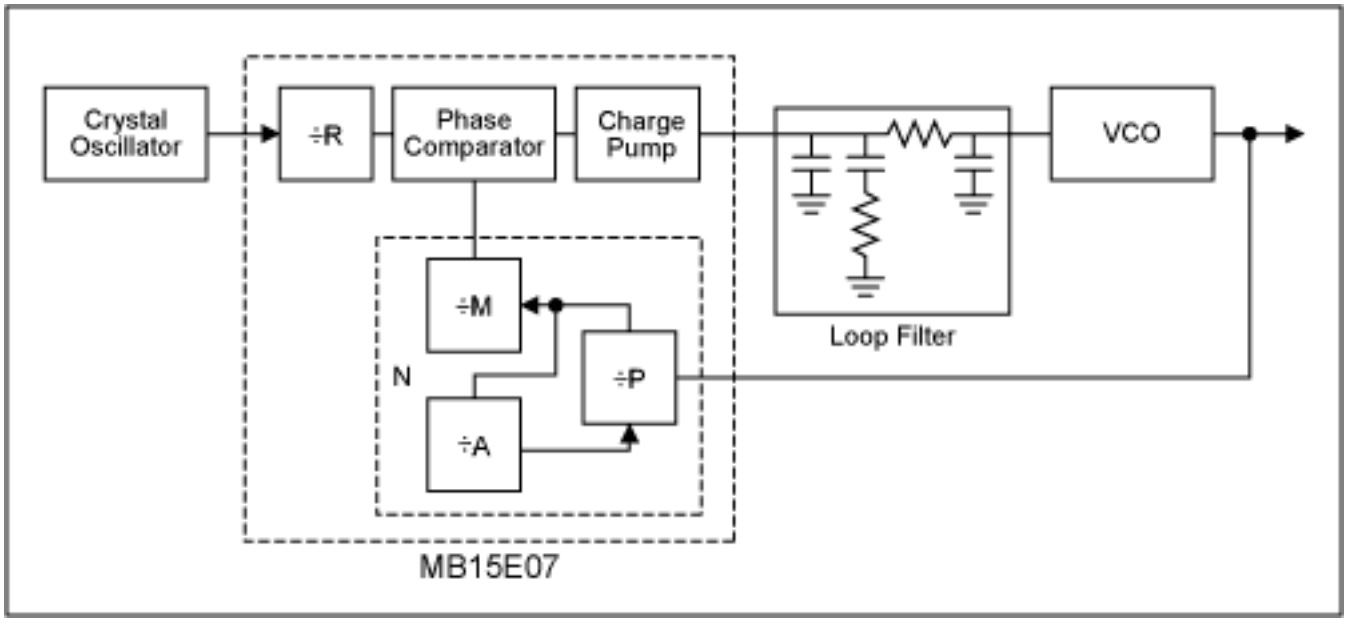

Figure 7. Simplified block diagram of a typical PLL system consisting of a PLL, crystal oscillator, loop filter, and VCO.

During power-up (assuming that the PLL was preprogrammed), the VCO would oscillate at the

desired frequency plus some offset. This frequency is first divided by the integer N, and then compared to the reference crystal oscillator frequency, whose frequency has also been divided by an integer R. If there is a phase difference between the two frequencies, the voltage at the PLL output changes accordingly. For example, if the VCO frequency is lower than that of the reference, the charge-pump will charge the loop filter capacitors to increase the voltage. If the VCO frequency is higher than the reference, the charge-pump will discharge the loop filter capacitors to decrease the voltage. An increase in voltage results in an increase in frequency, and visa versa. Hence, the PLL functions as a feedback loop that keeps the VCO output frequency locked at the desired frequency. The VCO frequency is a function of N, R and f_{REF} and is calculated as follows:

$$f_{VCO} = \frac{N}{R} f_{REF} \qquad \text{EQ. 15}$$

For example, if P = 32, M = 31, and A = 8, using EQ. 14, N counter is calculated to 1000. If the reference oscillator frequency is 20MHz and the R counter is set for 20, using EQ. 15, the VCO frequency is locked at 1000MHz.

Design Parameters

Careful design and implementation of the clock circuit is required to ensure optimum performance. This can be achieved by choosing the proper components and providing a well-designed high-frequency PC board. Table 1 shows the recommended component values for two different operating frequencies. These values ensure that the VCO will oscillate and phase lock at the desired frequency, while providing the proper output power levels. The output frequency of the MAX2620 is set by an external resonating tank, which consists of L1, C1, C2, C3, C4, and D1. L1, C1, C2, C3, and C4 set the free-running, oscillating frequency. The varactor diode, D1, fine-tunes the output frequency to the desired frequency. D1 is reverse biased and has a capacitance that varies with the bias voltage generated by the PLL output. A change in D1's capacitance allows for the fine-tuning of the output frequency.

The oscillating frequency can be calculated with the following equation:

$$f_O = \frac{1}{2\pi\sqrt{L1\left[C1 + \frac{C4 \cdot CD1}{C4 + CD1} + \frac{C2 \cdot C3}{C2 + C3}\right]}} \qquad \text{EQ. 16}$$

To accommodate the component tolerance, PCB, supply voltage, and temperature variations, the capacitance of D1 should be chosen such that the tuning range is about •}5% to •}10% from the nominal frequency. C4 is the capacitor that couples the varactor to the tuning tank. Increasing C4 can increase the tuning range. C2 and C3 are feedback capacitors necessary for

the oscillator to function properly. Typically, C2 = 2.7pF and C3 = 1.0pF. For 1.0GHz, chose L1 = 5.6nH, C4 = 4.7pF, and C1 = 1.0pF.

Both the VCO output and ADC clock input have to be matched to 50Ω. A LC network (L2 and C6) is used at the VCO output to ensure optimum power transfer to the clock input of the ADC. The matching network has a bandpass-filter-like frequency response that further reduces the thermal noise floor.

Table 1. Suggested Component Values for the Clock Generator

Designation	Description	
	f_{out} = 600MHz	f_{out} = 1000MHz
R1	240Ω	390Ω
R2	240Ω	390Ω
C1	1.0pF	1.0pF
C2	2.7pF	2.7pF
C3	1.0pF	1.0pF
C4	9.0pF	3.3pF
C5	9.0pF	2.2pF
C6	3.0pF	1.5pF
C7	12nF	3.9pF
C8	120nF	39nF
C9	12nF	3.9nF
L1	12nH (±2%)	5.6nH (±2%)
L2	18nH	10nH
D1	SMV1233-001 (Alpha Industries)	SMV1233-001 (Alpha Industries)

The charge pump output of the PLL pulses at the phase comparison frequency determined by R and the external crystal oscillator. A loop filter is employed to filter these pulses into a constant DC-control voltage for the VCO. The third-order loop filter (Figure 2) consists of C7, C8, C9, R1 and R2. Use simplified EQ. 17 to 23 to calculate the component values [3].

$$\text{LoopBandwidth} = f_{Loop} \le \frac{f_{comparison}}{20} \qquad \text{EQ. 17}$$

$$f_n = \frac{f_{Loop}}{\pi\left(\xi + \frac{1}{4\xi}\right)} \quad \text{EQ. 18}$$

$$C8 = \frac{I_{CP}K_{VCO}}{N(2\pi f_n)^2} \quad \text{EQ. 19}$$

$$C7 = \frac{C8}{10} \quad \text{EQ. 20}$$

$$R1 = 2\xi\sqrt{\frac{N}{I_{CP}K_{VCO}C8}} \quad \text{EQ. 21}$$

$$R1 = R2 \quad \text{EQ. 22}$$

$$C9 = \frac{C8}{10} \quad \text{EQ. 23}$$

N = The counter value from EQ. 14
ξ = Damping factor, typically 0.707
I_{CP}= The charge pump current, 10mA for the MB15E07
K_{VCO}= The VCO tuning gain or sensitivity

The VCO tuning gain, K_{VCO}, depends on the component values used in the VCO tank. The VCO tuning gain in this design example is about 35MHz/V.

The MB15E07 is programmed via the SPI™compatible interface. Table 2 shows the register/counter settings for 600MHz (MAX106) and 1000MHz (MAX104) operation:

Table 2. Suggested Register Settings for the MB15E07 with 20MHz Crystal Oscillator

	600MHz	1000MHz
$f_{COMPARISON}$	500kHz	1000kHz
Loop Bandwidth	25kHz	50kHz
R Counter	40	20

P Counter	32	32
M Counter	37	31
A Counter	16	8
SW bit	HIGH	HIGH
FC bit	HIGH	HIGH

To ensure good high-frequency PC board layout, keep the following suggestions in mind:

- Keep all PC board trace lengths as short as possible. Design with controlled impedance traces.
- Choose the smallest component size possible, preferably type 0603 or 0402.
- Use high quality-factor (Q) components to minimize VCO phase noise and maximize output power transfer. A Q factor of 40 or greater should be sufficient.
- Keep all the components for the resonating tank circuit as close together and as close to the MAX2620 as possible.
- Place de-coupling capacitors close to the VCO, and with a direct connection to the ground plane. All V_{CC}connections should have their own de-coupling capacitors.
- Maintain a 50Ω connection between the VCO output and the ADC clock input.
- Use component value recommendations from Table 1 as a starting point. Possible parasitic effects may require fine-tuning of some component values to ensure optimal performance.

Experimental Results

To demonstrate the performance of the proposed clock circuit, designed from the suggested equations and techniques, the circuit in Figure 2 was designed and tested with the MAX104 evaluation kit. Figure 6 shows the output of the proposed high-frequency, low jitter clock measured with a spectrum analyzer. The oscillation frequency is phase locked at 1GHz, with an output level of -2dBm. Figure 8 shows the signal-to-noise ratio of the MAX104 ADC over analog input frequency. With f_{SAMPLE} = 1.0GHz and f_{IN} at -1dBFS, the SNR varies from 47.1dB to 45.5dB for analog frequencies ranging from 10MHz to 1GHz, respectively. Compared to a known low-jitter signal generator (HP8662A), the SNR measured with the proposed clock is only ~0.4dB lower.

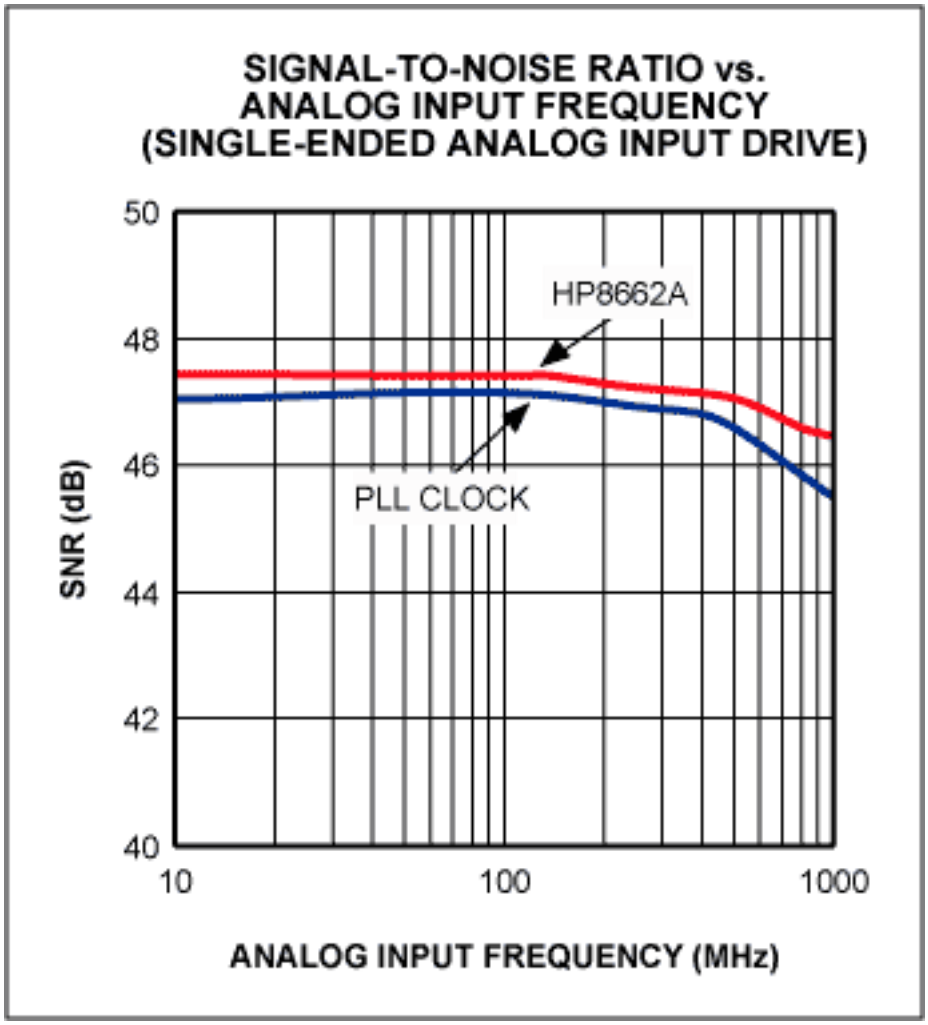

Figure 8. The SNR of the MAX104 is approximately 0.4dB lower with the PLL clock than with the HP8662A.

References:

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A similar version of this article appeared in the September 2001 issue of *Sensors* magazine.

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More Information

MAX104: QuickView -- Full (PDF) Data Sheet

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MAX106: QuickView -- Full (PDF) Data Sheet

MAX107: QuickView -- Full (PDF) Data Sheet -- Free Samples

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